

What is claimed is:

1 1. A method comprising:
2 receiving a data sequence in a receiver having a
3 plurality of lanes;
4 detecting a predetermined character in the data
5 sequence in a first lane; and
6 tracking a time period until the predetermined
7 character is detected in the plurality of lanes.

1 2. The method of claim 1, further comprising
2 resetting the receiver if a predetermined number of cycles
3 is exceeded before the predetermined character is detected
4 in the plurality of lanes.

1 3. The method of claim 1, further comprising
2 realigning the data sequence based on when the
3 predetermined character is detected in each of the
4 plurality of lanes.

1 4. The method of claim 3, further comprising
2 transmitting the realigned data sequence from the receiver
3 after the predetermined character is detected in the
4 plurality of lanes.

1 5. The method of claim 3, further comprising
2 determining whether the predetermined character is received
3 simultaneously on the plurality of lanes.

1 6. The method of claim 1, wherein the data sequence
2 comprises a training sequence.

1 7. The method of claim 1, wherein the data sequence
2 is byte striped.

1 8. A method comprising:
2 receiving data packets on a plurality of channels of a
3 receiver;
4 determining whether the data packets are misaligned
5 while the data packets are maintained in buffers
6 corresponding to the plurality of channels; and
7 aligning the data packets if the data packets are
8 misaligned.

1 9. The method of claim 8, wherein determining
2 whether the data packets are misaligned comprises analyzing
3 whether a predetermined value is received on each of the
4 plurality of channels within a first time period.

1 10. The method of claim 8, further comprising
2 transmitting the data packets in an aligned manner.

1 11. The method of claim 10, further comprising
2 holding the data packets until each of the buffers has a
3 predefined depth.

1 12. The method of claim 8, further comprising
2 realigning the data packets if the data packets become
3 misaligned.

1 13. The method of claim 8, wherein the data packets
2 are byte striped.

1 14. An apparatus comprising:
2 buffers to store data packets from a plurality of
3 channels; and
4 a state machine coupled to the buffers to deskew the
5 data packets while the data packets are stored in the
6 buffers.

1 15. The apparatus of claim 14, wherein the state
2 machine is adapted to hold the data packets in the buffers
3 until a predetermined character is present in each of the
4 buffers.

1 16. The apparatus of claim 15, further comprising a
2 counter to count cycles occurring after receipt of a first
3 data packet having the predetermined character.

1 17. The apparatus of claim 14, further comprising a
2 plurality of state machines, each corresponding to one of
3 the plurality of channels.

1 18. The apparatus of claim 14, wherein the data
2 packets comprise InfiniBand data packets.

1 19. An article comprising a machine-readable storage
2 medium containing instructions that if executed enable a
3 system to:

4 receive a data sequence in a receiver having a
5 plurality of lanes;

6 detect a predetermined character in the data sequence
7 in a first lane; and

8 track a time period until the predetermined character
9 is detected in the plurality of lanes.

1 20. The article of claim 19, further comprising
2 instructions that if executed enable the system to reset
3 the receiver if a predetermined number of cycles is
4 exceeded before the predetermined character is detected in
5 the plurality of lanes.

1 21. The article of claim 19, further comprising
2 instructions that if executed enable the system to
3 determine whether the data sequence is misaligned while the
4 data sequence is maintained in buffers corresponding to the
5 plurality of lanes.

1 22. A system comprising:
2 a switch fabric;
3 a plurality of buffers coupled to the switch fabric to
4 receive data packets from a plurality of channels; and
5 a state machine coupled to the plurality of buffers to
6 deskew the data packets while the data packets are received
7 in the plurality of buffers.

1 23. The system of claim 22, further comprising a host
2 channel adapter including the plurality of buffers.

1 24. The system of claim 23, wherein the host channel
2 adapter further includes a counter to count cycles
3 occurring after receipt of a first data packet having a
4 predetermined character.

1 25. The system of claim 22, wherein the switch fabric
2 comprises an InfiniBand switch fabric.